

S-LP7524DT3WG

60V P-Channel Power MOSFET

1. FEATURES

- High Efficiency
- Low Thermal Resistance
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S-prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.

2. APPLICATIONS

- Power Tools
- DC-DC Converter
- Motor Control

3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
LP7524DT3WG	LP7524	5000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		VDS	-60	V
Gate-to-Source Voltage		VGS	±20	V
Continuous Drain Current(Note 1)	TA=25°C	ID	-8.5	A
	TA=100°C		-5	
	TC=25°C		-43.5	
	TC=100°C		-27.5	
Continuous Drain Current(Note 3)	TA=25°C	ID	-4.8	A
	TA=100°C		-3	
Pulsed Drain Current (Note 2)		IDM	-34	A
Avalanche Current		IAS	26	A
Avalanche Energy(L=0.1mH)		EAS	33.8	mJ
Power Dissipation(Note 1)	TA=25°C	PD	2.5	W
	TC=25°C		62.5	
Power Dissipation(Note 3)		PD	1	W
Operating Junction and Storage Temperature Range		Tj/Tstg	-55~+150	°C

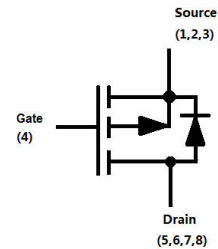
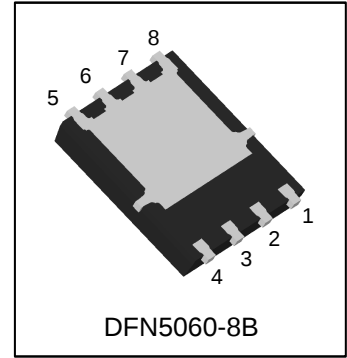
5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Junction-to-Ambient(Note 1)	RθJA	50	°C/W
Maximum Junction-to-Ambient(Note 3)	RθJA	117	
Maximum Junction-to-Case	RθJC	2	

1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

2.Pulse width limited by maximum junction temperature.

3.Surface mounted on FR4 board using the minimum recommended pad size.

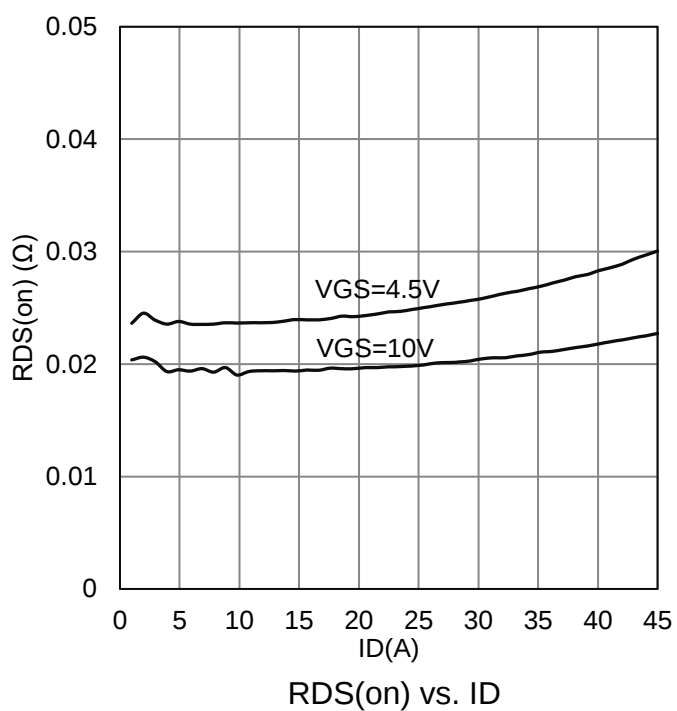
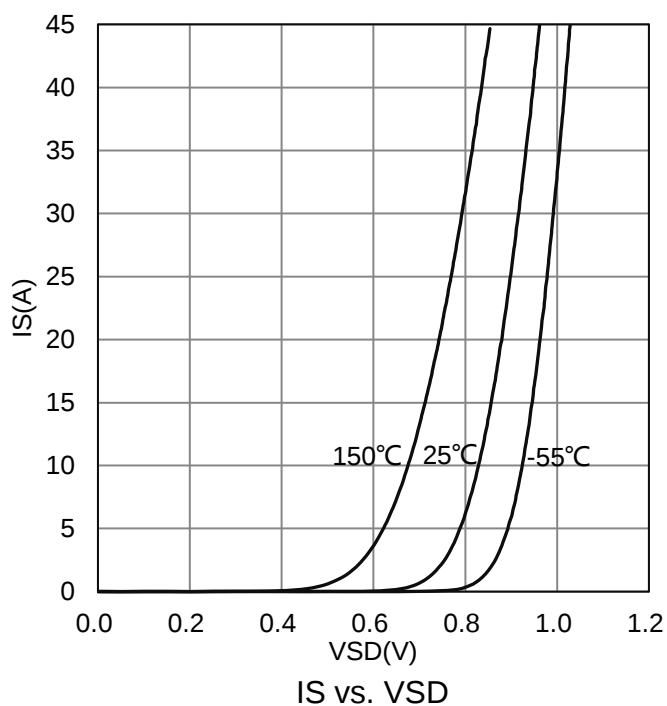
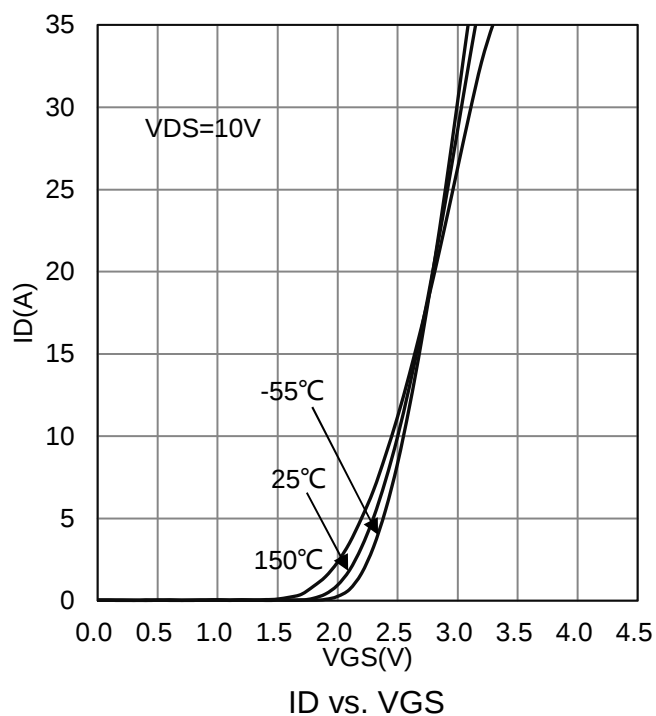
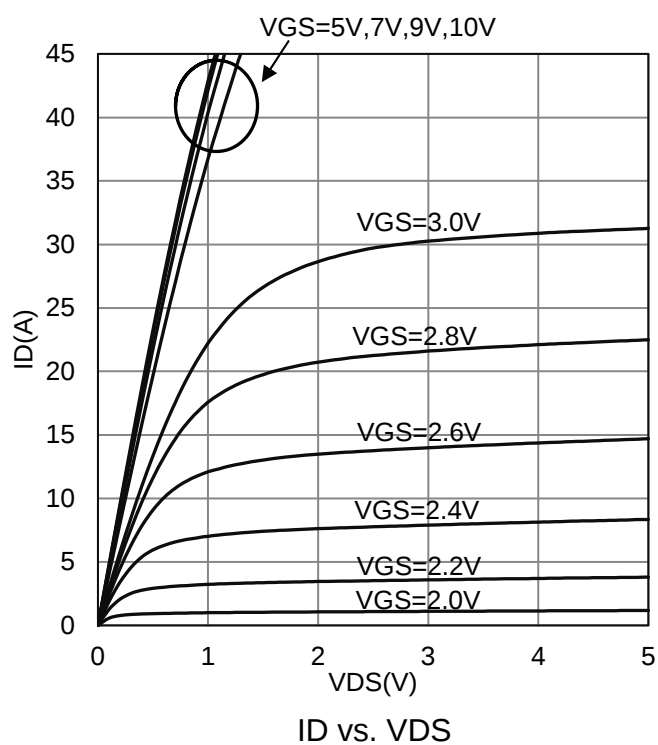


6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

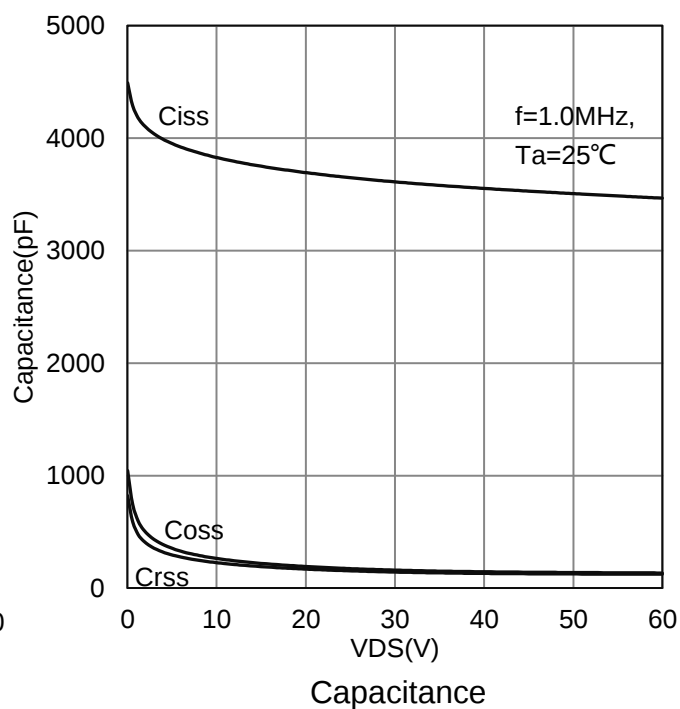
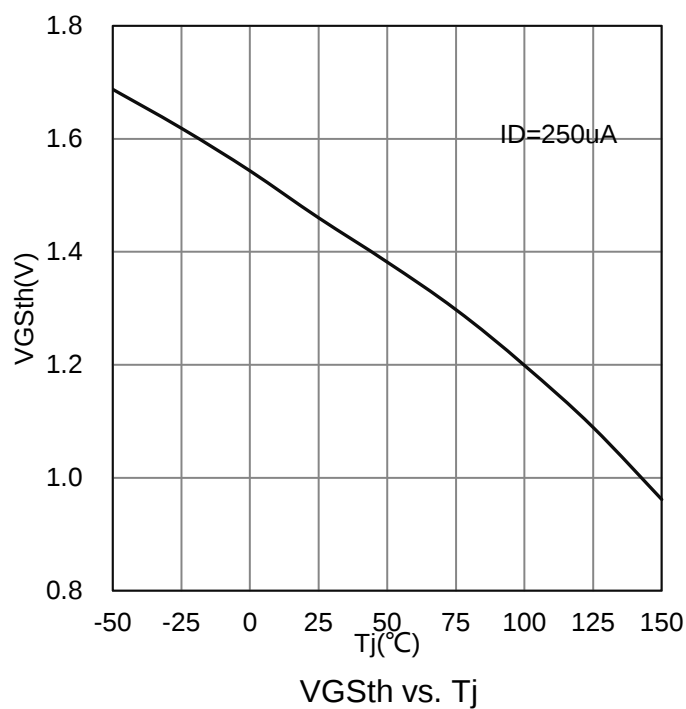
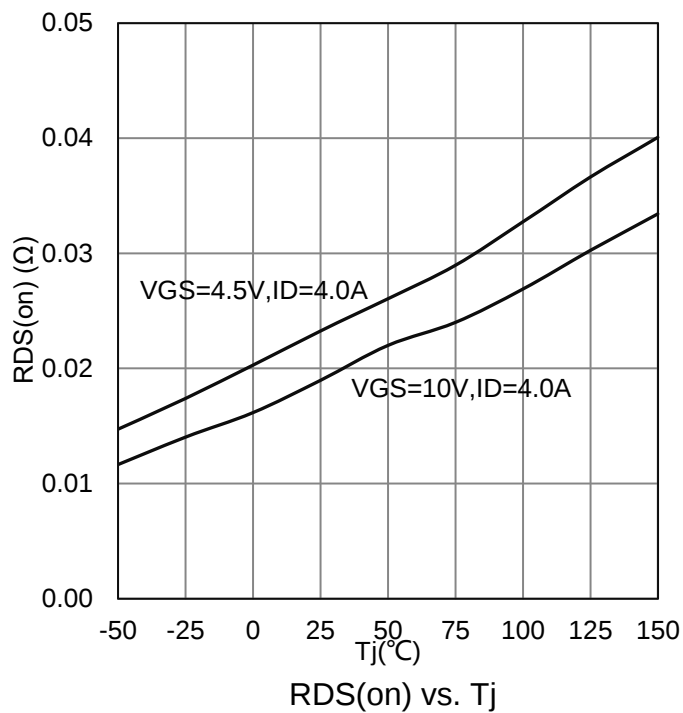
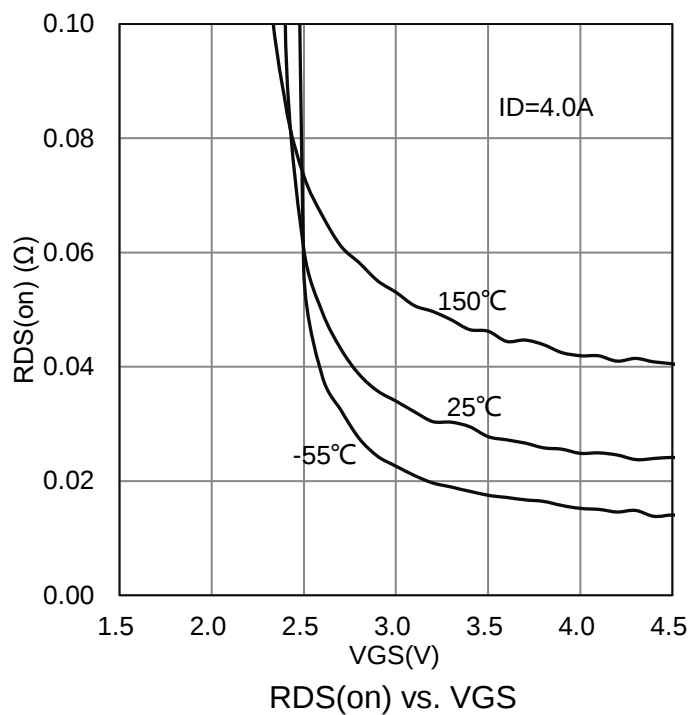
Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static						
Drain–Source Breakdown Voltage (VGS = 0 V, ID = -250 μ A)		VBRDSS	-60	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = -250 μ A)		VGS(th)	-1	-	-3	V
Gate Leakage Current (VDS = 0 V, VGS = $\pm$ 20 V)		IGSS	-	-	$\pm$ 10	μ A
Zero Gate Voltage Drain Current (VDS = -48 V, VGS = 0 V)		IDSS	-	-	-1	μ A
Drain-Source On-Resistance(Note 4) (VGS = -10 V, ID = -4 A) (VGS = -4.5 V, ID = -4 A)		RDS(ON)	- -	19 24	24 32	m Ω
Diode Forward Voltage (IS = -2 A, VGS = 0 V)		VSD	-	-	-1.2	V
Dynamic						
Total Gate Charge	(VDS = -30 V, VGS = -4.5 V, ID = -4 A)	Qg	-	29.6	-	nC
Gate-Source Charge		Qgs	-	7.4	-	
Gate-Drain Charge		Qgd	-	9.7	-	
Turn-On Delay Time	(VDS = -30 V, RL = 7.5 Ω , ID = -4 A, VGEN = -10 V, RGEN = 6 Ω)	td(on)	-	15	-	ns
Rise Time		tr	-	18	-	
Turn-Off Delay Time		td(off)	-	136	-	
Fall Time		tf	-	76	-	
Input Capacitance	(VDS = -30 V, VGS = 0 V, f = 1 MHz)	Ciss	-	3571	-	pF
Output Capacitance		Coss	-	162	-	
Reverse Transfer Capacitance		Crss	-	146	-	

3. Pulse test: PW $\leq$ 300 μ s duty cycle $\leq$ 2%.

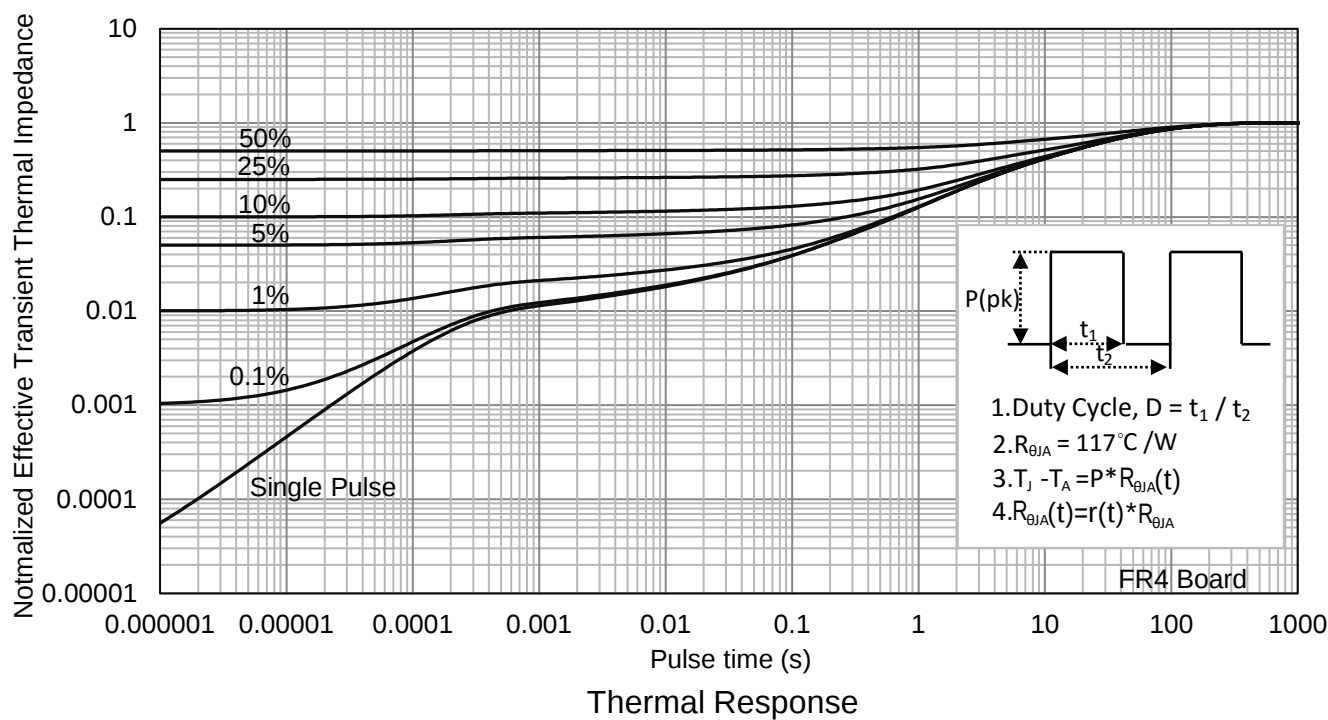
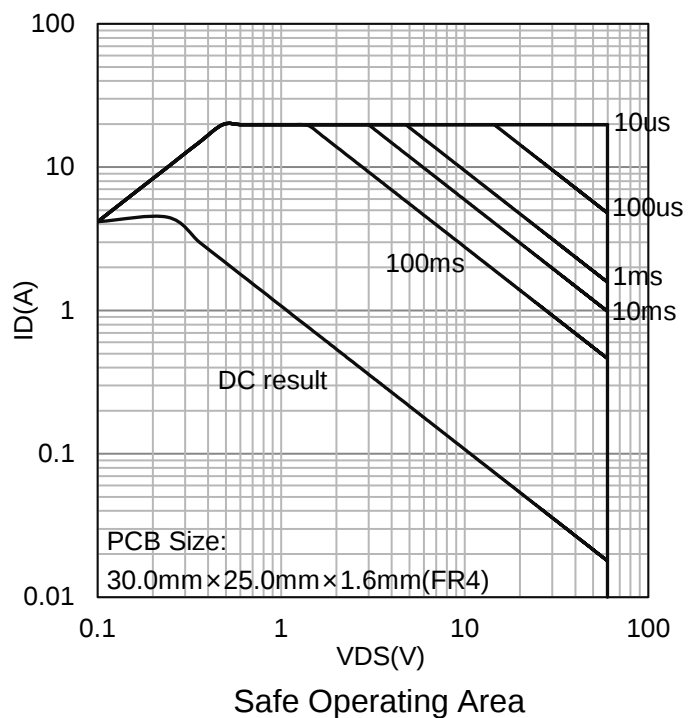
7. ELECTRICAL CHARACTERISTICS CURVES



7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

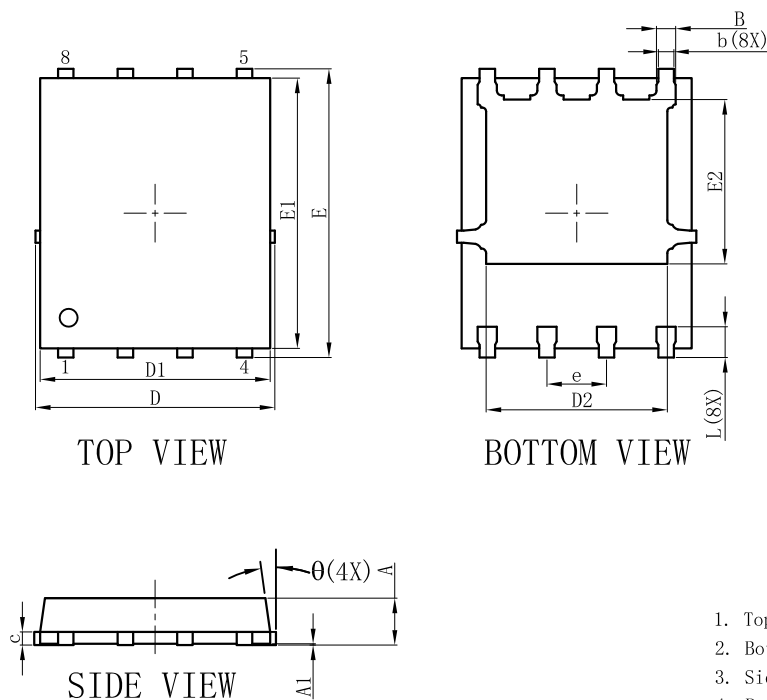


7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



8.OUTLINE AND DIMENSIONS

DFN5060-8B

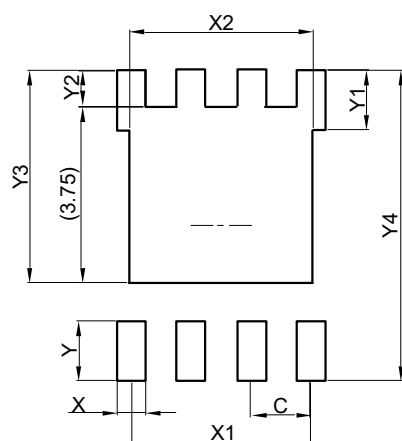


DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish $Ra0.4 \pm 0.2\mu m$
2. Bottom package surface finish $Ra0.7 \pm 0.2\mu m$
3. Side package surface finish $Ra0.4 \pm 0.2\mu m$
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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