

LN76076HDT1WG

N-Channel Power Trench MOSFET

1. FEATURES

- Max $R_{DS(on)}$ = 7.6 m Ω at V_{GS} = 10 V, I_D = 13 A
- Advanced Package and Silicon combination for low $R_{DS(on)}$ and high efficiency.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.

2. APPLICATIONS

- DC-DC Conversion

3. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Shipping
LN76076HDT1WG	LN76076H	3000/Tape&Reel

4. MAXIMUM RATINGS($T_a = 25^\circ\text{C}$)

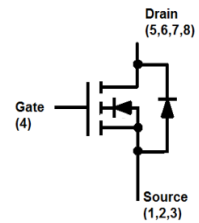
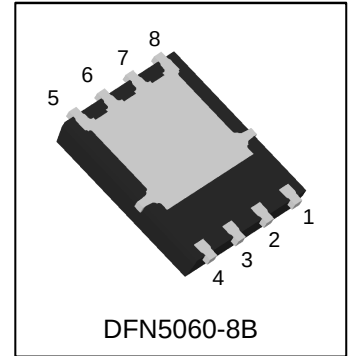
Parameter		Symbol	Limits	Unit
Drain-to-Source Voltage		V_{DS}	100	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current(Note 1)	$T_C = 25^\circ\text{C}$	I_D	74	A
	$T_A = 25^\circ\text{C}$		12	A
Pulsed Drain Current(Note 2)	$T_C = 25^\circ\text{C}$	I_{DM}	200	A
Avalanche Current		I_{AS}	34	A
Avalanche energy ($L=0.1\text{mH}$)		E_{AS}	57.8	mJ
Power Dissipation(Note 1)	$T_C = 25^\circ\text{C}$	P_D	104	W
	$T_A = 25^\circ\text{C}$		2.5	
Operating Junction and Storage Temperature Range		T_j/T_{stg}	$-55 \sim +150$	$^\circ\text{C}$

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Junction-to-Ambient(Note 1)	R_{thja}	50	$^\circ\text{C/W}$
Junction-to-Case	R_{thjc}	1.2	

1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.

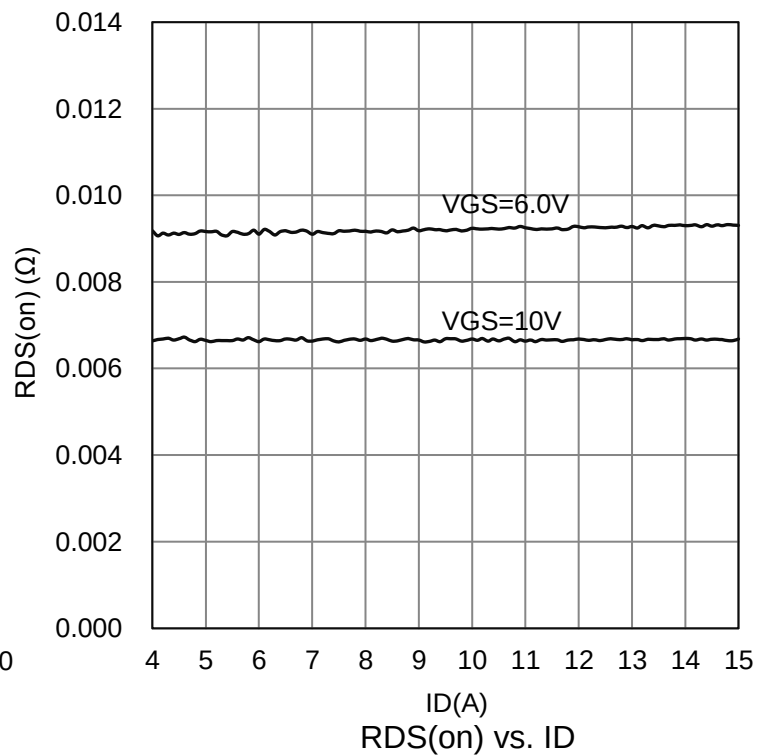
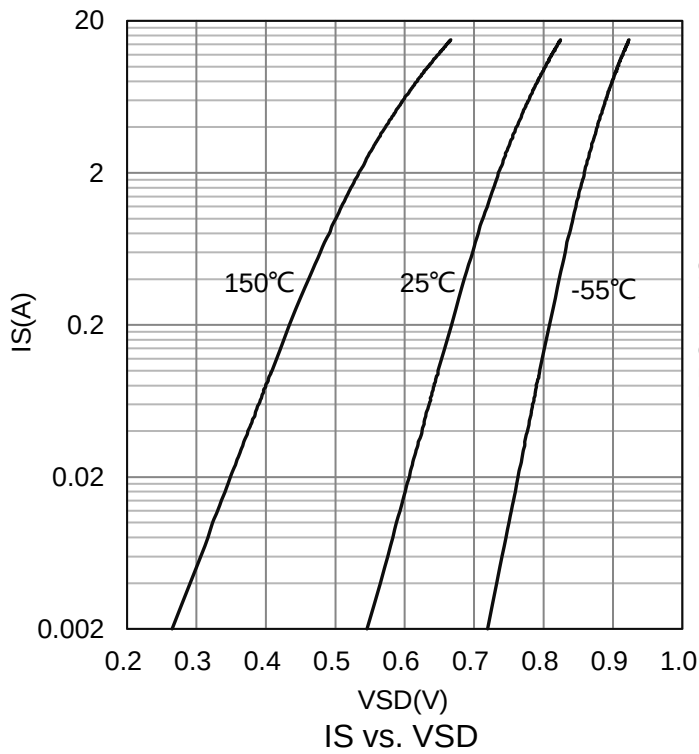
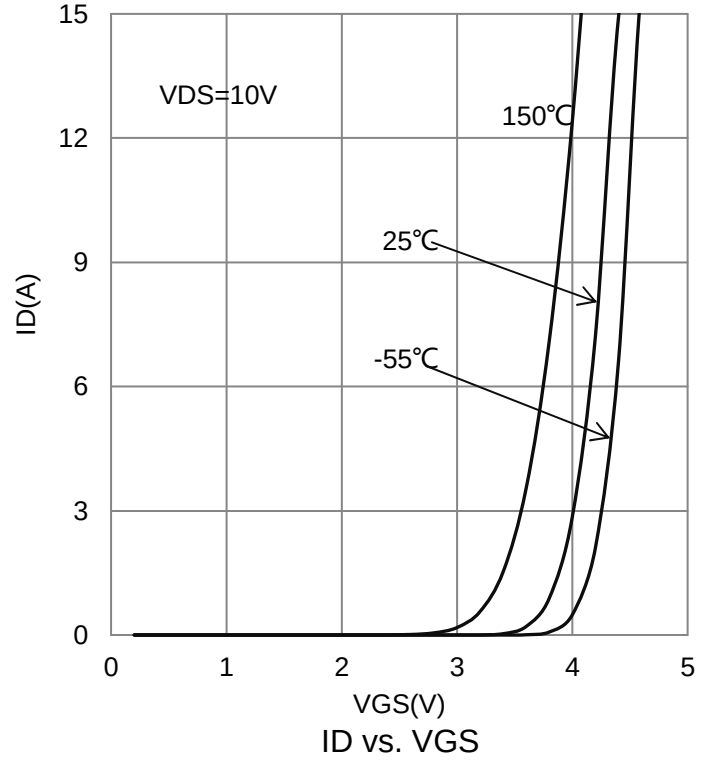
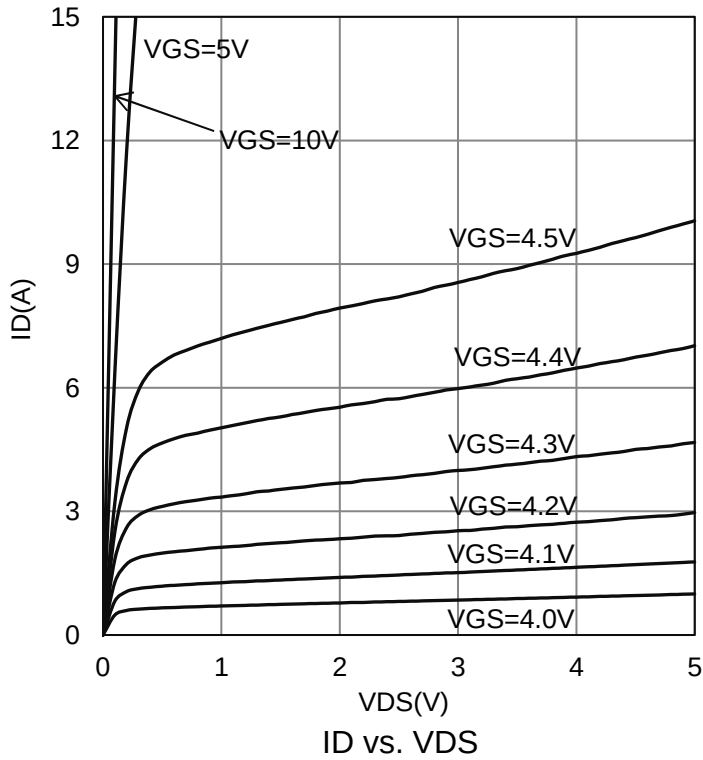
2.Pulse width limited by maximum junction temperature.



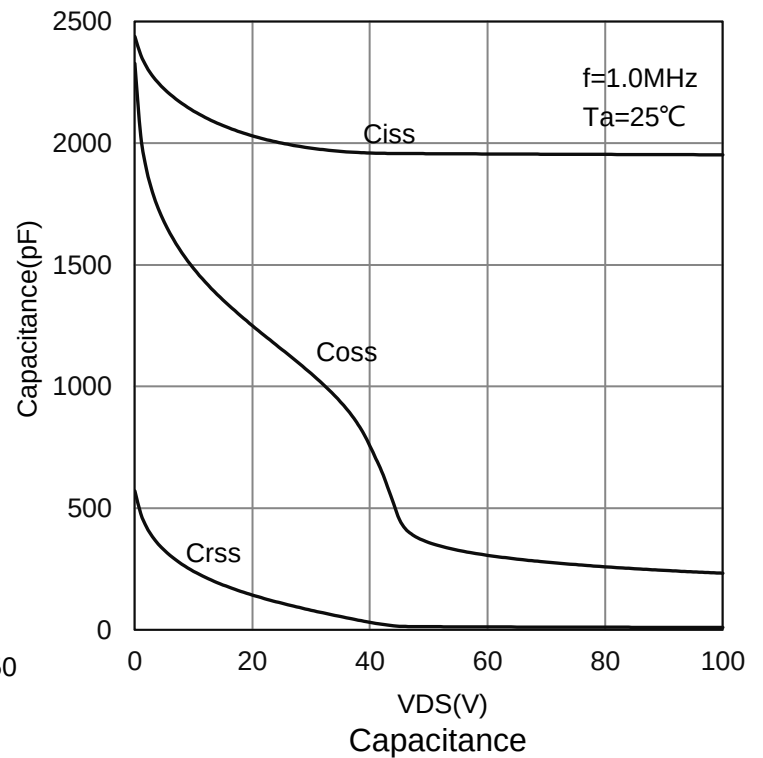
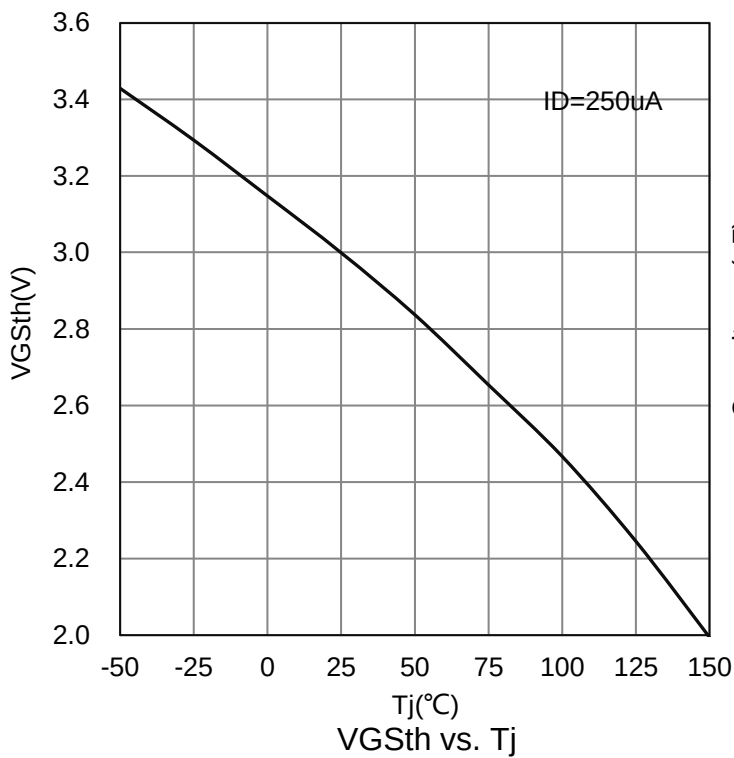
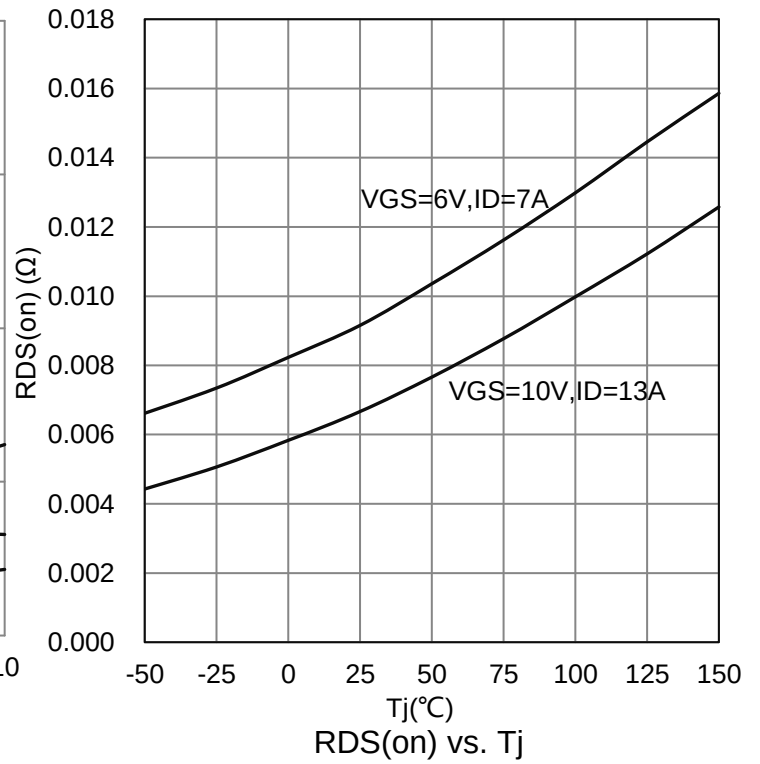
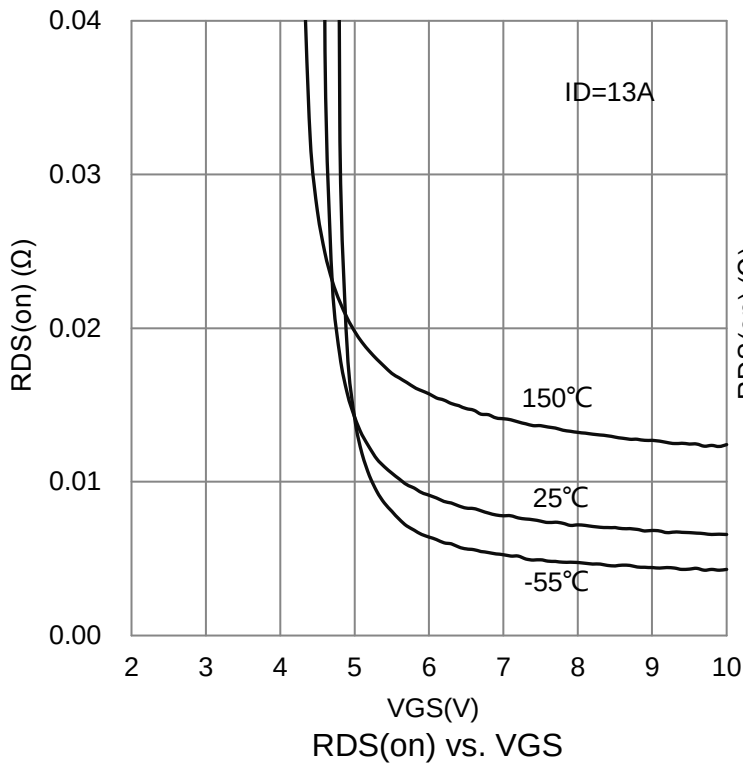
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
STATIC					
Drain to Source Breakdown Voltage (VGS =0V, ID =250μA)	VDSS	100	-	-	V
Drain-to-Source Leakage Current (VDS =80V, VGS =0V)	IDSS	-	-	800	nA
Gate-Body leakage current (VDS =0V, VGS = ±20V)	IGSS	-	-	±100	nA
Gate Threshold Voltage (VDS = VGS , ID = 250μA)	VGS(th)	2	2.8	4	V
Drain-to-Source On-Resistance (VGS = 10 V, ID = 13 A) (VGS = 6 V, ID = 7 A)	RDS(ON)	- -	6.2 9	7.6 12	mΩ
Diode Forward Voltage (VGS = 0 V, IS = 2.1 A) (VGS = 0 V, IS = 13 A)	VSD	- -	0.7 0.8	1.2 1.3	V
DYNAMIC					
Total Gate Charge (VGS=5 V)	(ID =13A,VDS =50V)	Qg	-	20.1	nC
Total Gate Charge (VGS=10 V)		Qg	-	32.9	
Gate to Source Charge		Qgs	-	7	
Gate to Drain Charge		Qgd	-	11.3	
Turn-on Delay Time	(VDD = 50V, ID = 13A, RG = 6 Ω,VGS = 10V)	td(on)	-	15	nS
Rise Time		tr	-	8	
Turn-Off Delay Time		td(off)	-	23	
Fall Time		tf	-	7	
Input Capacitance	(VGS = 0V ,VDS = 50V, f = 1MHz)	Ciss	-	1957	pF
Output Capacitance		Coss	-	359	
Reverse Transfer Capacitance		Crss	-	13.2	

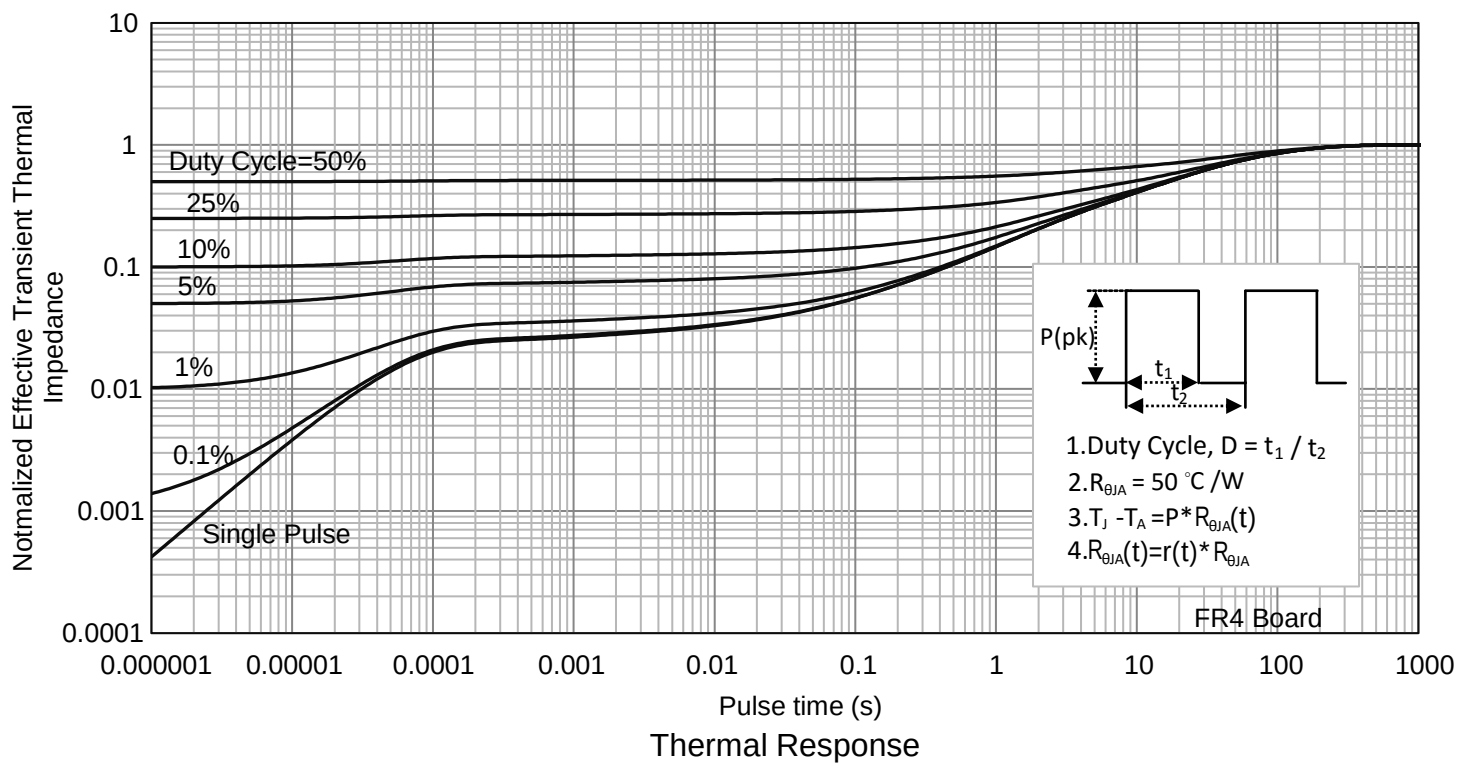
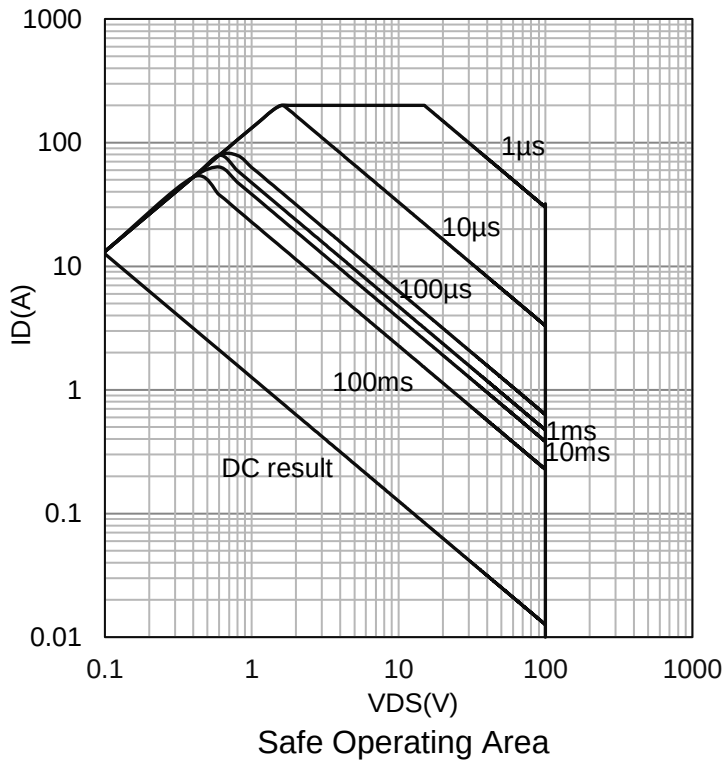
7. ELECTRICAL CHARACTERISTICS CURVES



7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

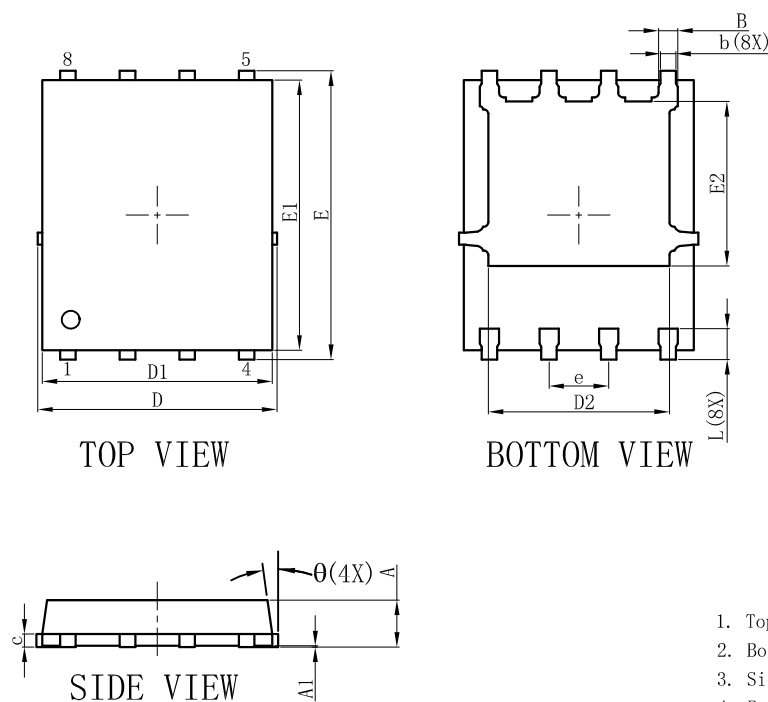


7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



8.OUTLINE AND DIMENSIONS

DFN5060-8B

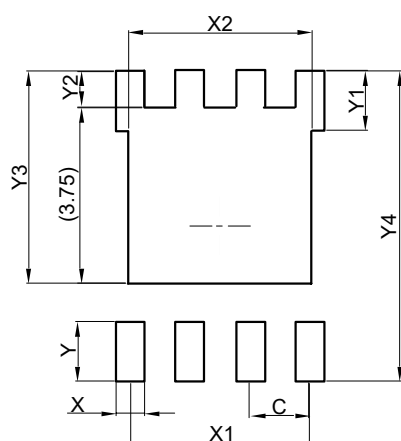


DFN5060-8B			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.00	0.02	0.05
E	6.00	6.15	6.30
E1	5.66	5.76	5.86
E2	3.40	3.50	3.60
D	4.95	5.10	5.25
D1	4.80	4.90	5.00
D2	3.76	3.86	3.96
b	0.30	0.35	0.40
B	0.36	0.41	0.46
L	0.56	0.66	0.76
e	1.27BSC		
c	0.254REF.		
θ	0°	-	12°
All Dimensions in mm			

GENERAL NOTES

1. Top package surface finish $Ra0.4 \pm 0.2\mu m$
2. Bottom package surface finish $Ra0.7 \pm 0.2\mu m$
3. Side package surface finish $Ra0.4 \pm 0.2\mu m$
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

9.SOLDERING FOOTPRINT



DFN5060-8B	
DIM	(mm)
C	1.27
X	0.61
X1	3.81
X2	3.91
Y	1.27
Y1	1.27
Y2	0.77
Y3	4.52
Y4	6.61

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