

Bias Resistor Transistor

PNP Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

• Applications

Inverter, Interface, Driver

• Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on / off conditions need to be set for operation, making the device design easy.

- We declare that the material of product compliance with RoHS requirements.

- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

• Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V _{CC}	-50	V
Input voltage	V _{IN}	-40 to +10	V
Output current	I _C	-500	mA
Power dissipation	P _D	200	mW
Junction temperature	T _J	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

DEVICE MARKING AND RESISTOR VALUES

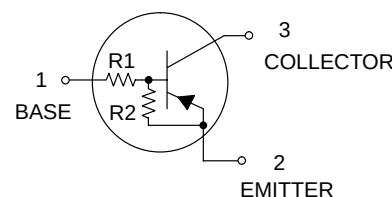
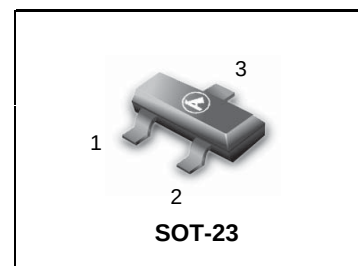
Device	Marking	R1 (K)	R2 (K)	Shipping
LDTB114ELT1G S-LDTB114ELT1G	F14	10	10	3000/Tape & Reel
LDTB114ELT3G S-LDTB114ELT3G	F14	10	10	13000/Tape & Reel

• Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input voltage	V _{I(off)}	-	-	-0.5	V	V _{CC} =-5V, I _O =-100μA
	V _{I(on)}	-3	-	-		V _O =-0.3V, I _O =-10mA
Output voltage	V _{O(on)}	-	-0.1	-0.3	V	I _O /I _I =-50mA/-2.5mA
Input current	I _I	-	-	-0.88	mA	V _I =-5V
Output current	I _{O(off)}	-	-	-0.5	μA	V _{CC} =-50V, V _I =0V
DC current gain	G _I	56	-	-	-	V _O =-5V, I _O =-50mA
Input resistance	R _I	7	10	13	kΩ	-
Resistance ratio	R ₂ /R ₁	0.8	1	1.2	-	-
Transition frequency	f _T *	-	200	-	MHz	V _{CE} =-10V, I _E =50mA, f=100MHz

* Characteristics of built-in transistor

LDTB114ELT1G
S-LDTB114ELT1G



LDTB114ELT1G;S-LDTB114ELT1G

●Electrical characteristic curves

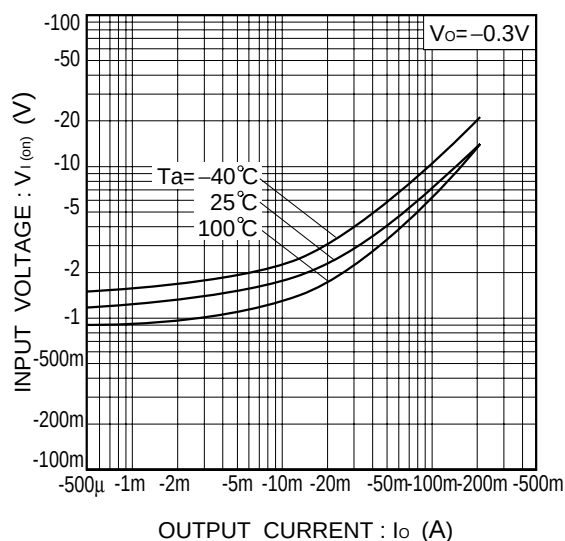


Fig.1 Input voltage vs. output current (ON characteristics)

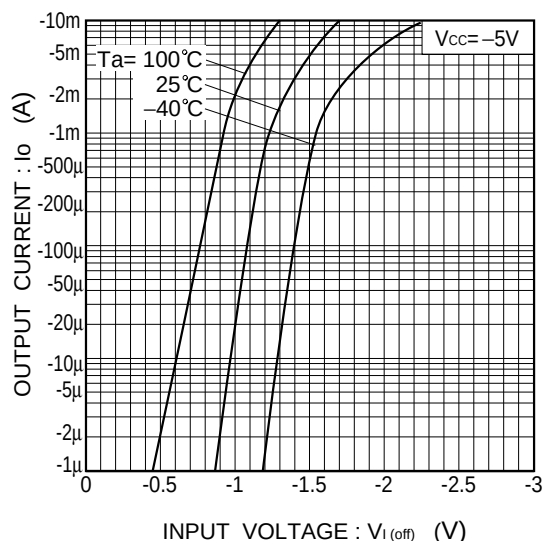


Fig.2 Output current vs. input voltage (OFF characteristics)

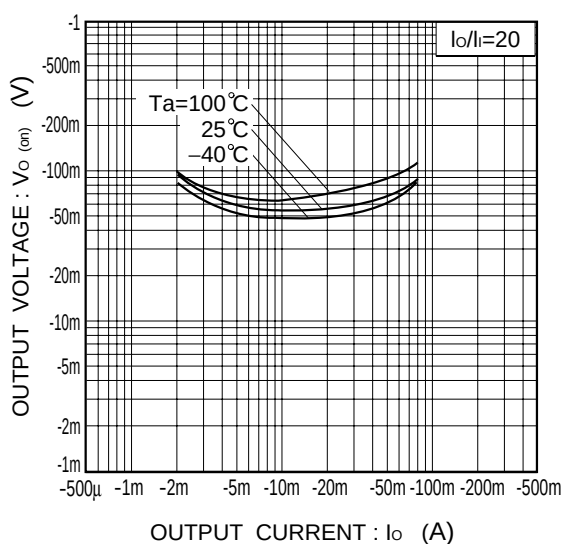


Fig.4 Output voltage vs. output current

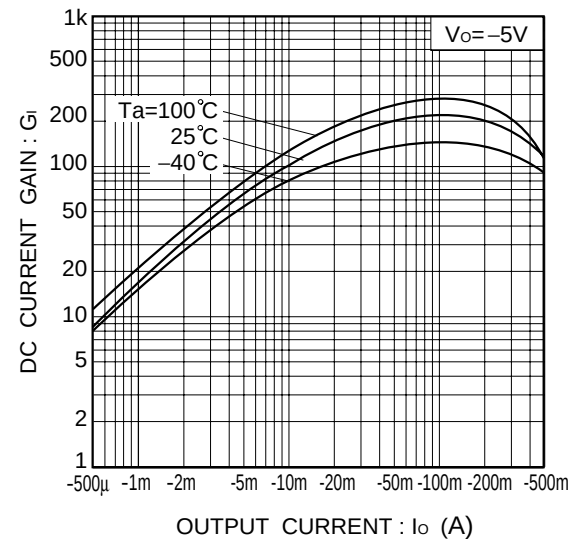
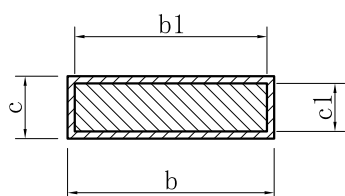
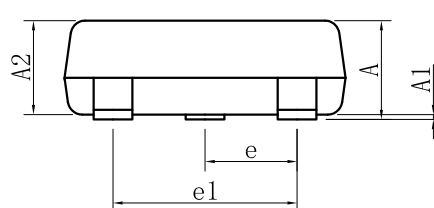
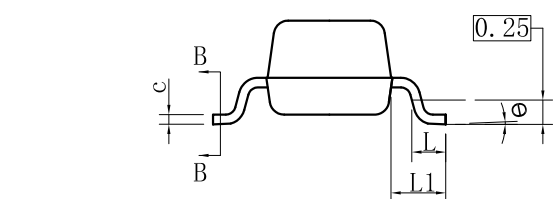


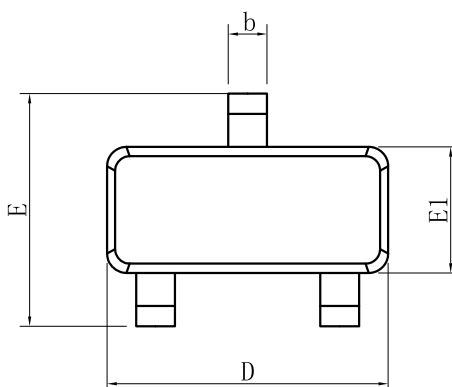
Fig.3 DC current gain vs. output current

LDTB114ELT1G;S-LDTB114ELT1G

OUTLINE AND DIMENSIONS



SECTION B-B

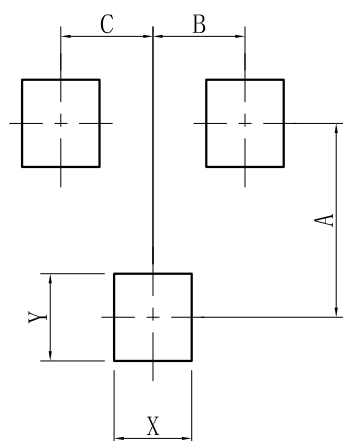


SOT23			
DIM	MIN	NOR	MAX
A	0.89	—	1.12
A1	0.01	—	0.10
A2	0.88	0.95	1.02
b	0.30	—	0.50
b1	0.30	0.40	0.45
c	0.08	—	0.20
c1	0.08	0.10	0.16
D	2.80	2.90	3.04
E	2.10	—	2.64
E1	1.20	1.30	1.40
e	0.95BSC		
e1	1.90BSC		
L	0.40	0.46	0.60
L1	0.54REF		
θ	0°	—	8°
All Dimensions in mm			

GENERAL NOTES

- 1.Top package surface finish $Ra0.4 \pm 0.2\mu m$
- 2.Bottom package surface finish $Ra0.7 \pm 0.2\mu m$
- 3.Side package surface finish $Ra0.4 \pm 0.2\mu m$

SOLDERING FOOTPRINT



SOT-23	
DIM	(mm)
X	0.80
Y	0.90
A	2.00
B	0.95
C	0.95

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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