

Bias Resistor Transistor

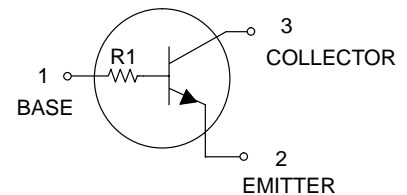
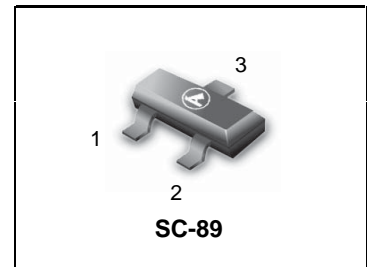
NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

LDTC114YET1G

- **Applications**
Inverter, Interface, Driver

- **Features**
 - 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
 - 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
 - 3) Only the on/off conditions need to be set for operation, making the device design easy.

- We declare that the material of product compliance with RoHS requirements.



● **Absolute maximum ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V _{CB0}	50	V
Collector-emitter voltage	V _{CE0}	50	V
Emitter-base voltage	V _{EB0}	5	V
Collector current	I _C	70	mA
Collector power dissipation	P _C	200	mW
Junction temperature	T _J	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
LDTC114YET1G	N14	10	47	3000/Tape & Reel
LDTC114YET3G	N14	10	47	10000/Tape & Reel

● **Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input voltage	V _{I(off)}	-	-	0.3	V	V _{CC} =5V, I _O =100μA
	V _{I(on)}	1.4	-	-		V _O =0.3V, I _O =1mA
Output voltage	V _{O(on)}	-	0.1	0.3	V	I _O /I _I =5mA/0.25mA
Input current	I _I	-	-	0.88	mA	V _I =5V
Output current	I _{O(off)}	-	-	0.5	μA	V _{CC} =50V, V _I =0V
DC current gain	G _I	68	-	-	-	V _O =5V, I _O =5mA
Input resistance	R ₁	7	10	13	kΩ	-
Resistance ratio	R ₂ /R ₁	3.7	4.7	5.7	-	-
Transition frequency	f _r *	-	250	-	MHz	V _{CE} =10V, I _E =-5mA, f=100MHz

* Characteristics of built-in transistor

LDTC114YET1G

●Electrical characteristic curves

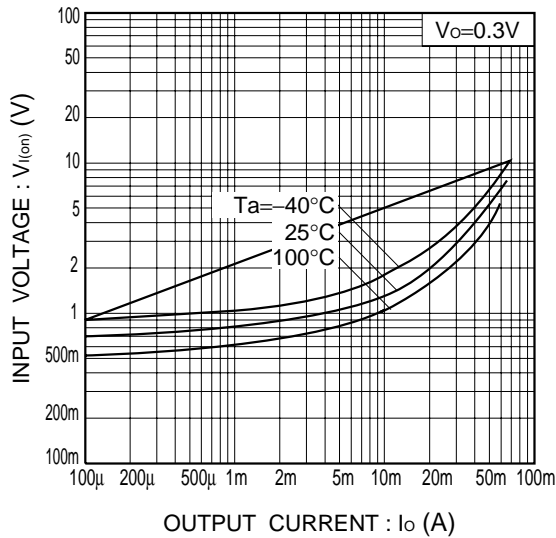


Fig.1 Input voltage vs. output current (ON characteristics)

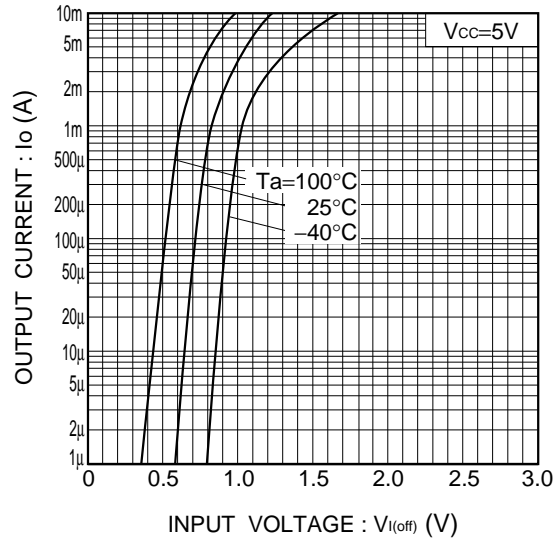


Fig.2 Output current vs. input voltage (OFF characteristics)

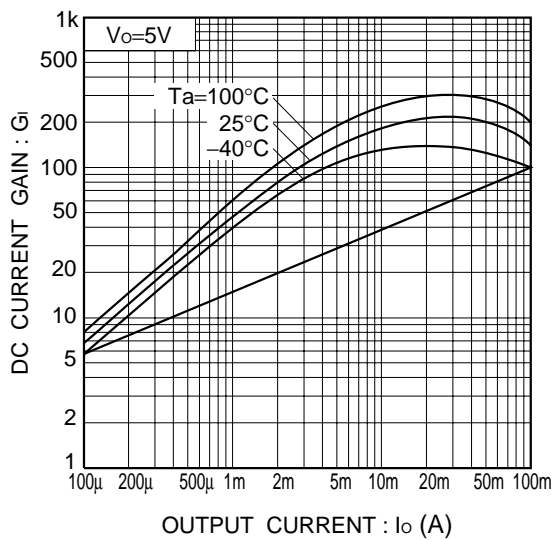


Fig.3 DC current gain vs. output current

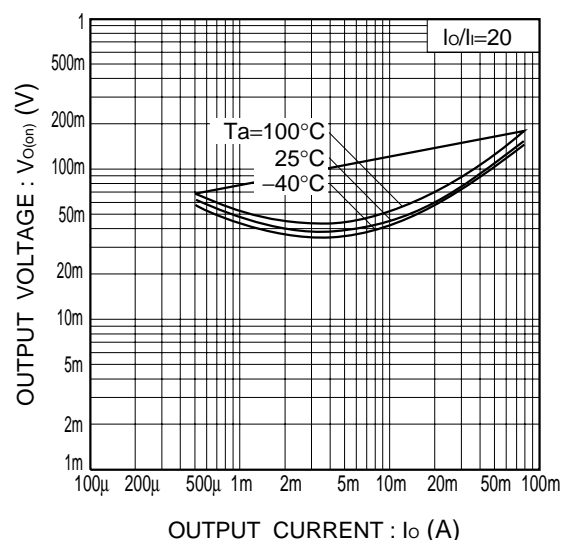
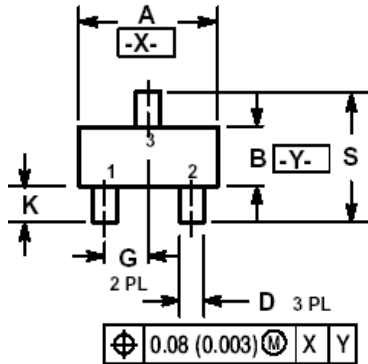
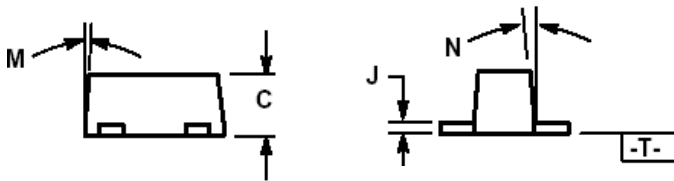


Fig.4 Output voltage vs. output current

LDTC114YET1G
SC-89

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067

